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Comparative Performance Analysis of Nonlinearity Cancellation Techniques for MOS-C Realization in Integrator Circuits

Hasan Çiçekli, Ahmet Gökçen, Uğur Çam

Abstract**—**In this paper, a comparative performance analysis of mostly used four nonlinearity cancellation techniques used to realize the passive resistor by MOS transistors, is presented. The comparison is done by using an integrator circuit which is employing sequentially Op-amp, OTRA and ICCII as active element. All of the circuits are implemented by MOS-C realization and simulated by PSPICE program using 0.35µm process TSMC MOSIS model parameters. With MOS-C realization, the circuits became electronically tunable and fully integrable which is very important in IC design. The output waveforms, frequency responses, THD analysis results and features of the nonlinearity cancellation techniques are also given.

Keywords**—**Integrator circuits, MOS-C realization, nonlinearity cancellation, tunable resistors.

I. Introduction

INTEGRATED CIRCUIT (IC) design becomes more popular with the advances in analog VLSI technology. In IC, the resistors are one of its components. Resistors can be designed and fabricated in semiconductor processing. Resistors which are fabricated as physical resistors occupy large area and they increase the chip space. Also, they have large sheet resistance and large parasitic capacitance, and that limits their applications in high frequency circuits. Resistors which are synthesized by using MOS transistors can provide large resistance values, and they occupy smaller area in chip space. In this respect, it could be attractive to implement the resistors using MOS transistors and this would reduce the chip size considerably. Also, transistors consume less power than resistors and resistors suffer from temperature effect. However, resistor implementation by MOS transistors occur linear and nonlinear terms in transistor current. The main problem is cancelling these nonlinear terms in the transistor current. In the literature there are many techniques presented to cancel these nonlinear terms [1]. Using these techniques, MOS transistors can be used as linear resistor. The resultant resistor value can be tuned electronically by the gate voltage of the MOS transistor [2]-[6].

An n-channel MOSFET is shown in Fig. 1. The device's gate is connected to a DC control voltage V_C and the substrate is connected to a fixed dc bias V_B [1].

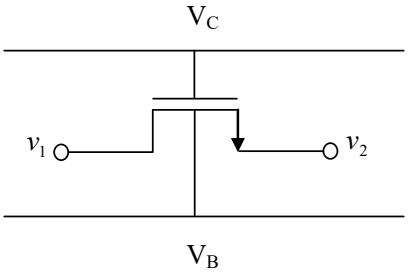

Fig. 1 A n-channel MOSFET

To allow operation in the "non-saturation" region, the terminal voltages are assumed to remain below V_C by at least an amount V_K as shown in Fig. 2. Also, v_1 and v_2 are assumed to remain above V_B by a non-critical quantity V_Q [1].

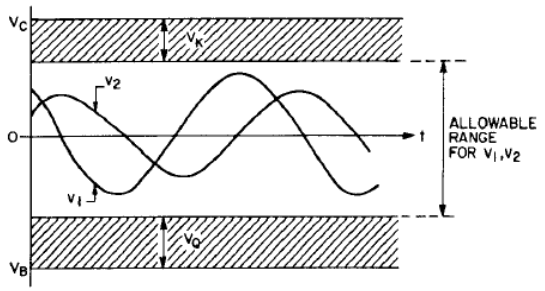

Fig. 2 Terminal voltages for the transistor [1]

A model for the MOS transistor is shown in Fig. 3.

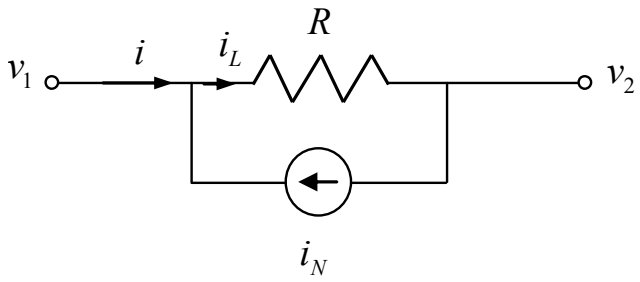

Fig. 3 Low frequency large signal model for the MOS transistor

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The transistor current *i* can be written in the following form:

$$i = i_L - i_N \tag{1}$$

where, i_N and i_L depict nonlinear and linear terms, respectively.

The linear term of the transistor current can be defined as:

$$i_L = G(v_1 - v_2) \tag{2}$$

In (2), the conductance parameter G is given by:

$$G = \left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_{TB}) \tag{3}$$

where *W* and *L* are channel width and length respectively, μ is effective mobility, C_{ox} is oxide capacitance per unit area, V_{TB} is threshold voltage of the transistor. Clearly, if one cancels the effect of the i_N, the transistor behaves like a linear resistor with a conductance. The resistance *R=1/G* can be written in the following form:

$$R = \left(\frac{L}{W}\right)R_S \tag{4}$$

where L/W is aspect ratio of the transistor which is a design parameter, and R_S is given by:

$$R_S = \frac{1}{\mu C_{ox}(V_C - V_{TB})} \tag{5}$$

The above material holds also for p-channel devices, with appropriate changes in the signs of voltages and currents.

The nonlinear term in (1) can be written in the following form:

$$i_N = g(v_1) - g(v_2) \tag{6}$$

where the function *g(v)* is independent of V_C can be written as:

$$g(v) = g_e(v) + g_o(v) \tag{7}$$

where $g_e(v)$ and $g_o(v)$ are even and odd functions, respectively and can be written as:

$$g_e(v) = \left(\frac{W}{L}\right)\mu C_{ox}\left\{\frac{1}{2}v^2 + \frac{1}{3}\gamma\left[(V_R + v)^{3/2} + (V_R - v)^{3/2}\right]\right\} \tag{8}$$

$$g_o(v) = \left(\frac{W}{L}\right)\mu C_{ox}\left\{\gamma\left[\frac{1}{3}(V_R + v)^{3/2} - \frac{1}{3}(V_R - v)^{3/2} - V_R^{1/2}v\right]\right\} \tag{9}$$

where γ is body effect coefficient.

The nonlinear term of the current i can be written using (6) and (7) as the following form:

$$i_N = g_e(v_1) + g_o(v_1) - g_e(v_2) - g_o(v_2) \tag{10}$$

$$i_N = [g_e(v_1) - g_e(v_2)] + [g_o(v_1) - g_o(v_2)] \tag{11}$$

The nonlinear term is:

$$i_N = \left[\left(\frac{W}{L}\right)\mu C_{ox}\left\{\frac{1}{2}v_1^2 + \frac{1}{3}\gamma(V_R + v_1)^{3/2} + \frac{1}{3}\gamma(V_R - v_1)^{3/2}\right\} - \left(\frac{W}{L}\right)\mu C_{ox}\left\{\frac{1}{2}v_2^2 + \frac{1}{3}\gamma(V_R + v_2)^{3/2} + \frac{1}{3}\gamma(V_R - v_2)^{3/2}\right\}\right] + \left[\left(\frac{W}{L}\right)\mu C_{ox}\left\{\frac{1}{3}\gamma(V_R + v_1)^{3/2} - \frac{1}{3}\gamma(V_R - v_1)^{3/2} - \gamma V_R^{1/2}v_1\right\} - \left(\frac{W}{L}\right)\mu C_{ox}\left\{\frac{1}{3}\gamma(V_R + v_2)^{3/2} - \frac{1}{3}\gamma(V_R - v_2)^{3/2} - \gamma V_R^{1/2}v_2\right\}\right] \tag{12}$$

After the simplification of the (12), i_N is:

$$i_N = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}(V_1^2 - V_2^2) + \frac{2}{3}\gamma(V_R + V_1)^{3/2} - \frac{2}{3}\gamma(V_R + V_2)^{3/2} - \gamma V_R^{1/2}(V_1 - V_2)\right] \tag{13}$$

Nonlinear current of transistor depicts even $[g_e(v_1) - g_e(v_2)]$ and odd $[g_o(v_1) - g_o(v_2)]$ components of expression. The term, $[g_e(v_1) - g_e(v_2)]$ is very small when compared to the linear term i_L. The term, $[g_o(v_1) - g_o(v_2)]$ depending on v_1 and v_2 is can be large and its effect must be eliminated.

II. Nonlinearity Cancellation of Transistor Current

Many different techniques have been proposed for eliminating the effect of nonlinearities. Some cancel the nonlinearities in the current of one device, while others cancel the nonlinearities in the difference or sum of the currents in two or more devices.

A. First Technique for Nonlinearity Cancellation

This technique uses a NMOS transistor which operates in non-saturation region. Drain and source of the NMOS transistor is connected to equal but opposite voltages as shown in Fig. 4. The substrate is assumed connected to source so the body effect is neglecting.

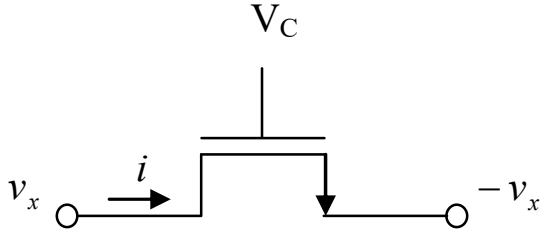

Fig. 4 First nonlinearity cancellation technique

The transistor current i can be written as; $i=i_L-i_N$. i_L and i_N had been calculated previously. For the first nonlinearity cancellation technique, i_N and i_L are defined as

$$i_N = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{2}{3}\gamma(V_R + V_x)^{3/2} - \frac{2}{3}\gamma(V_R - V_x)^{3/2} - \gamma V_R^{1/2} 2v_x\right] \quad (14)$$

$$i_L = \left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_{TB})2v_x \quad (15)$$

V_{TB} is the threshold voltage of the transistor and defined as

$$V_{TB} = V_{FB} + \phi_B + \gamma V_R^{1/2}, \quad (16)$$

where V_{FB} is flat-band voltage and $\emptyset_B$ is the surface inversion potential. The transistor current i can be written as

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\{(V_C - V_{FB} - \phi_B)(2v_x)\} - \frac{2}{3}\gamma\left[(V_R + V_x)^{3/2} - (V_R - V_x)^{3/2}\right] \quad (17)$$

By neglecting nonlinear terms, the following equation can be obtained:

$$i = \left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_{FB} - \phi_B)(2v_x) \quad (18)$$

The resistance value of the transistor can be calculated as:

$$R = \frac{2v_x}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_{FB} - \phi_B)} \quad (19)$$

$$R = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_{TB})} \quad (20)$$

The other non-linearity cancellation techniques achieved using same calculations are given below.

B. Second Technique for Nonlinearity Cancellation

In this technique, two NMOS transistors are used which each drain and source is connected to equal voltages as it is shown in Fig. 5.

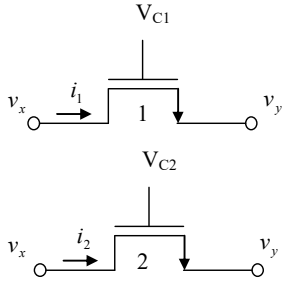

Fig. 5 Second nonlinearity cancellation technique

Each transistor has own control voltage. The currents of the transistors are:

$$i_1 - i_2 = [i_{L1} - i_{L2}] - [i_{N1} - i_{N2}] \quad (21)$$

After writing the linear and nonlinear terms of the current using (6) and (7) and doing required calculations, the resistance value of the NMOS transistors is obtained as:

$$R = \frac{(v_x - v_y)}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}(V_{C1} - V_{C2})} \quad (22)$$

C. Third Technique for Nonlinearity Cancellation

Another technique for nonlinearity cancellation which is shown in Fig. 6 consists of four NMOS transistors. The transistors have different control voltages which are V_{C1} and V_{C2} as it is seen in Fig. 6.

The current of the transistors is:

$$i - i' = [(i_{L1} + i_{L2}) - (i_{L3} + i_{L4})] - [(i_{N1} + i_{N2}) - (i_{N3} + i_{N4})] \quad (23)$$

Substituting linear and nonlinear terms into account and neglecting nonlinear terms, the transistor current i-i^1 is can be obtained as the following form:

$$i - i' = \left(\frac{W}{L}\right)\mu C_{ox}[2(V_{C1} - V_{C2})(v_x)] \quad (24)$$

$$i - i' = \left(\frac{1}{R_1} + \frac{1}{R_2}\right)2v_x \quad (25)$$

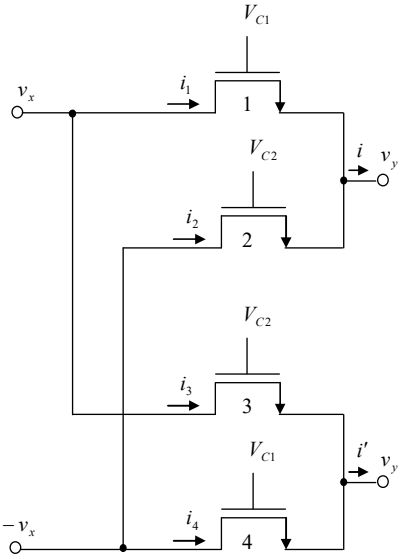

Fig. 6 Third nonlinear cancellation technique

The circuit which is shown in Fig. 6 achieves in principle complete cancellation of both even and odd nonlinearities. In this figure, R_1 and R_2 are resistance values.

D. Fourth Technique for Nonlinearity Cancellation

This technique is different from the others. The main difference is that keeping the bottom transistor on, the circuit necessitate the use of "depletion mode" devices (V_{TB}<0).

The other difference is that the expression for the resistance R for this circuit, in that V_{TB} should be replaced by $2V_{TB}$.

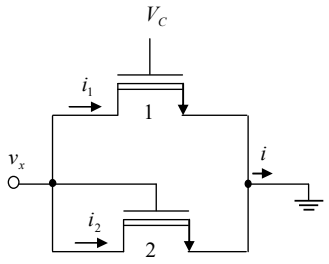

Fig. 7 Fourth nonlinear cancellation technique

The current of the transistors is:

$$i_1 + i_2 = \left[i_{L1} + i_{L2}\right] - \left[i_{N1} + i_{N2}\right] \tag{26}$$

After doing required calculations and neglecting the nonlinear terms, the resistance value obtained as:

$$R = \frac{v_x}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - 2V_{TB}\right)} \tag{27}$$

III. Performance Comparison

In this section, the performance comparison of mostly used four nonlinearity cancellation techniques which are mentioned is presented. The comparison is done by using an integrator circuit. All active and passive components except resistors, which will be implemented by MOS transistors, are assumed ideal. Thus, THD and frequency analysis of the MOS transistors can be compared. In all comparisons for integrators, the same input signal (V_{in}) having 0.1V amplitude and 500 kHz frequency is applied. The simulation is done using the PSPICE program and 0.35μm process TSMC MOSIS model parameters.

A. Op-Amp Based Integrators

1. Miller Integrator

The Miller integrator circuit is shown in Fig. 8.

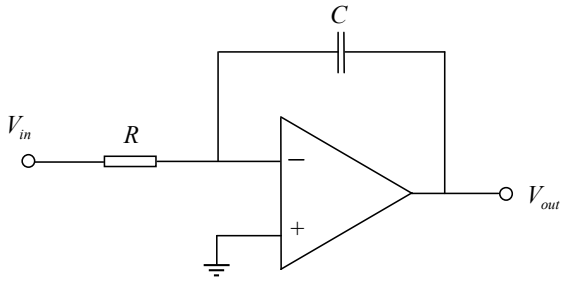

Fig. 8 Miller integrator

For the ideal integrator, the output voltage is can be written as:

$$V_{out} = -\frac{1}{RC}\int V_{in}.dt \tag{28}$$

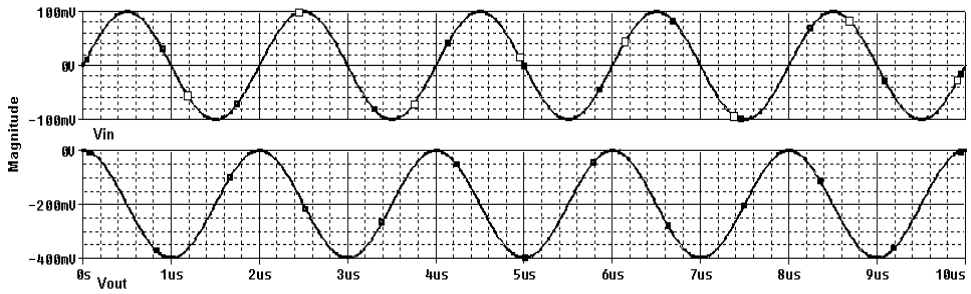

Fig. 9 Output waveform of Miller integrator with ideal R

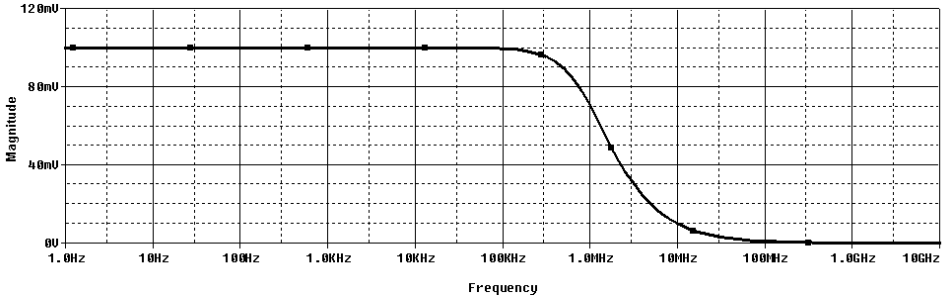

Fig. 10 Frequency response of Miller integrator with ideal R

Applying a sinusoidal signal to the integrator input, the obtained output waveform is depicted in Fig. 9. Fig. 10 shows the frequency response of the Miller integrator with unit gain.

The resistor in Fig. 8 can be implemented by using two NMOS transistors which are previously expressed in Fig. 7. Using fourth implementation technique, resistance value can be controlled via changing the V_C voltage. Thus integrator parameters can be controlled electronically. Fig. 11 shows the MOS-C realization of the Miller integrator with fourth nonlinearity cancellation technique [7].

Simulating MOS-C Miller integrator circuit which is shown in Fig. 11 with the input signal V_{in}, the obtained output waveform is shown in Fig. 12. The frequency response of the integrator with unit gain which is shown in Fig. 11 is depicted in Fig. 13.

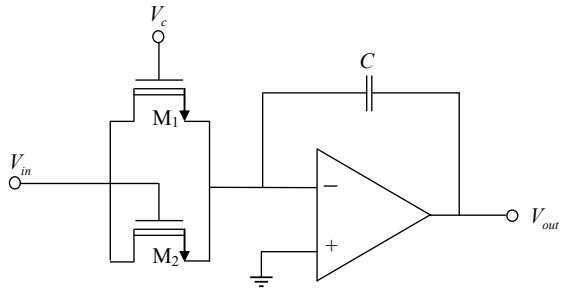

Fig. 11 MOS-C realization of Miller integrator [7]

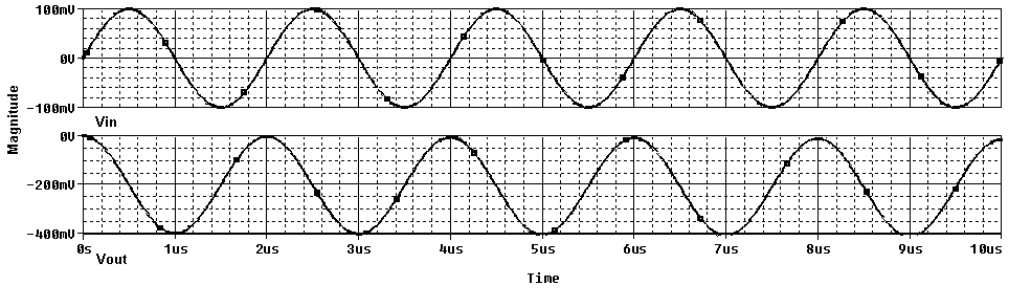

Fig. 12 Output waveform of MOS-C Miller integrator

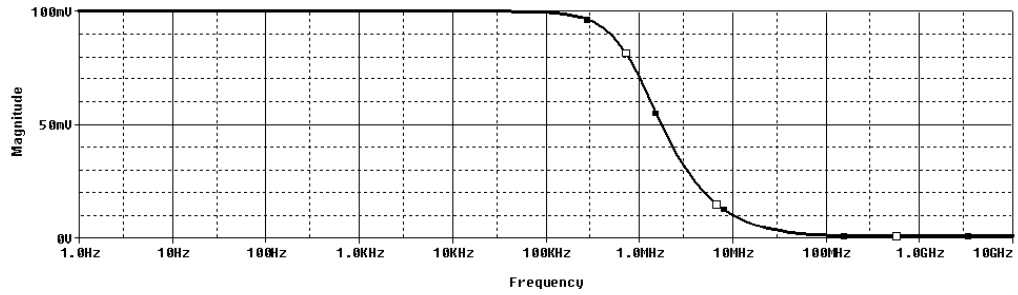

Fig. 13 Frequency response of Miller integrator

2. Op-Amp Integrator

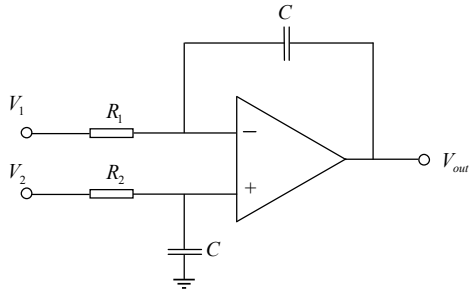

Fig. 14 Op-amp based integrator circuit

Another op-amp based integrator circuit is shown in Fig. 14 [8], [9]. The circuit consists of two resistors suitable for realization with four NMOS transistors, two capacitors and an op-amp as an active element.

If R_1 and R_2 are implemented by MOS transistors as previously mentioned in Section II *C*, then the resultant MOS-C integrator circuit becomes as shown in Fig. 15.

The resistance and thus integrator parameters can be tuned electronically by changing the gate voltages of NMOS transistors.

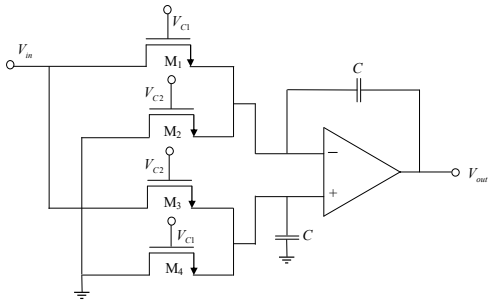

Fig. 15 MOS-C realization of Op-amp integrator circuit [9]

Fig. 16 shows the output waveform of the MOS-C Op-amp integrator circuit which is shown in Fig. 15. Fig. 17 shows the frequency response of the Op-amp integrator with unit gain.

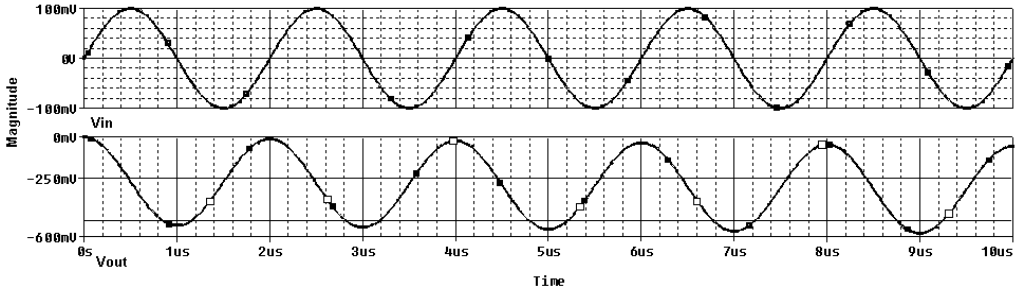

Fig. 16 Output waveform of the MOS-C Op-amp integrator

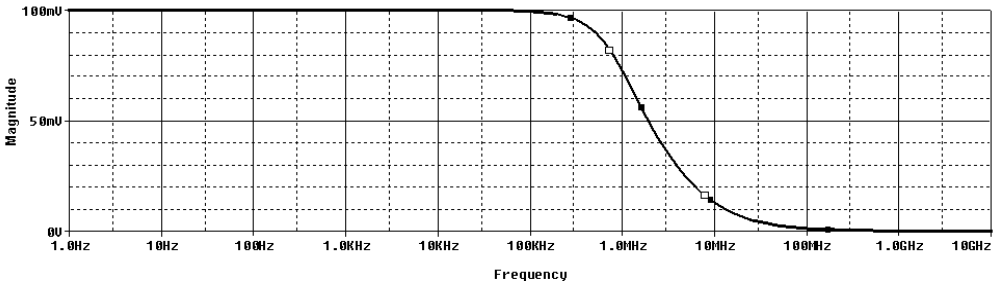

Fig. 17 Frequency response of Op-amp integrator

B. OTRA Based Integrator

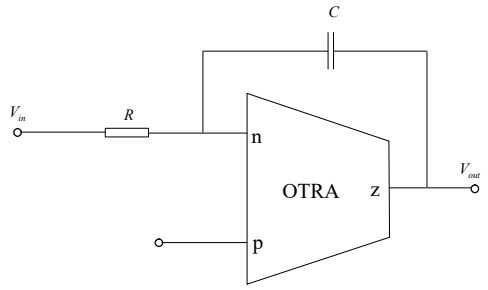

Fig. 18 OTRA based integrator

An OTRA based integrator is shown in Fig. 18. Implementing the resistor with two matched MOS transistors as mentioned previously, the OTRA based integrator circuit becomes as shown in Fig. 19. Thus, changing the gate voltages of the transistors, the tunable resistance and integrator parameters can be obtained [10].

Fig. 20 shows the output waveform of the MOS-C realization of OTRA based integrator with the input signal V_{in}. Fig. 21 shows the frequency response of the OTRA based integrator with unit gain.

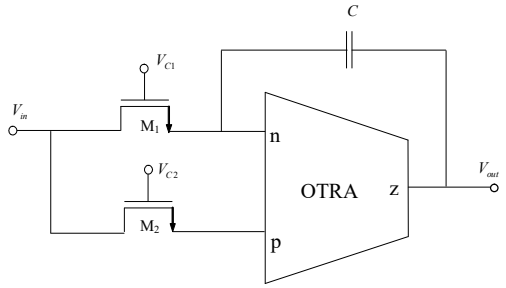

Fig. 19 MOS-C realization of OTRA based integrator

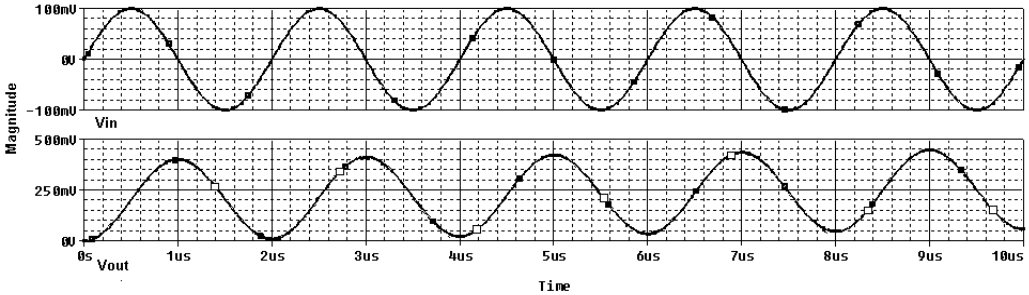

Fig. 20 Output waveform of MOS-C realization of OTRA based integrator

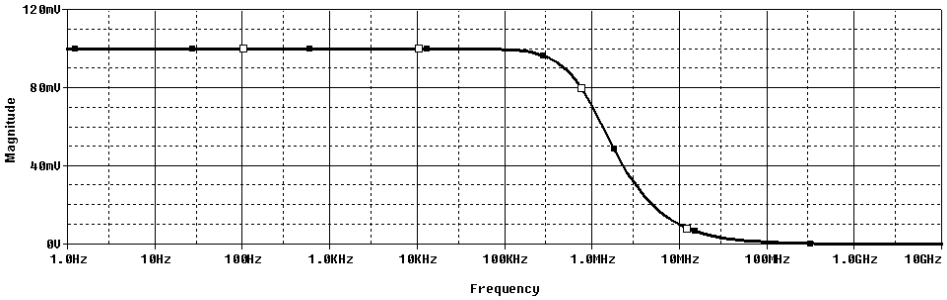

Fig. 21 Frequency response of OTRA based integrator

C. ICCII Based Integrator

An ICCII based integrator is shown in Fig. 22 [11].

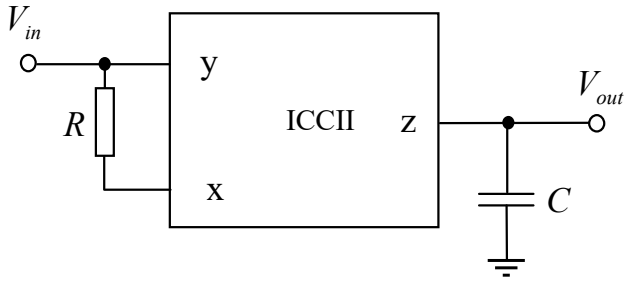

Fig. 22 ICCII based integrator

Taking into account of the input terminals of ICCII which have the same voltages with opposite signs, the resistor can be easily implemented by using a MOS transistor. The MOS-C realization of the ICCII based integrator is shown in Fig. 23.

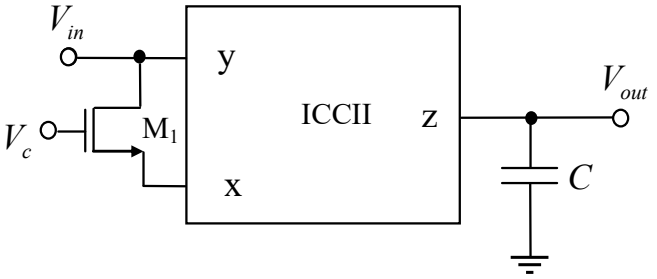

Fig. 23 MOS-C realization of ICCII based integrator

By changing the gate voltage of the NMOS transistor, electronically tuneable resistance and integrator parameters can be obtained. The output waveform of the MOS-C realization of ICCII based integrator is shown in Fig. 24.

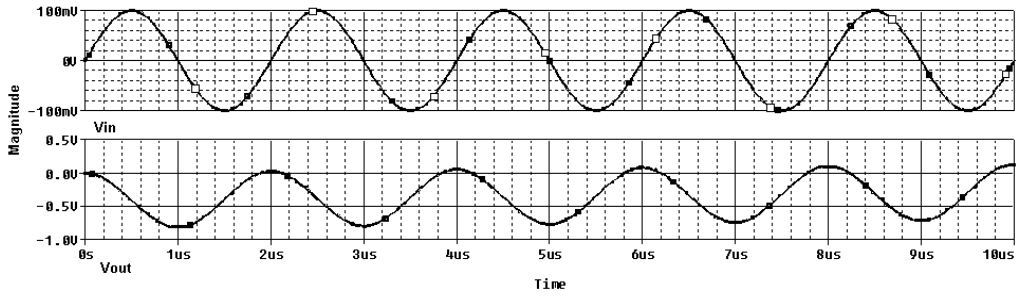

Fig. 24 Output waveform of MOS-C realization of ICCII based integrator

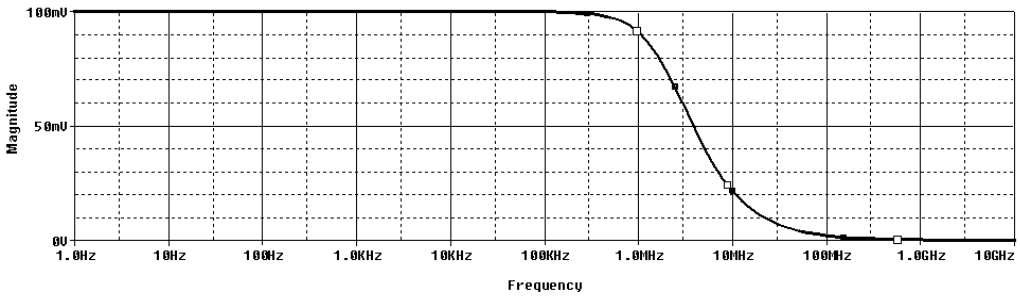

Fig. 25 Frequency response of ICCII based integrator

The frequency response of the ICCII based unit gain integrator is shown in Fig. 25. The total harmonic distortion

(THD) analysis results of the integrators which are mentioned above with the MOS-C realization techniques are given in Table I.

TABLE I
THD ANALYSIS OF THE MOS-C BASED INTEGRATOR AMPLIFIERS

	THD Analysis (%)
Miller integrator	0.30
Op-Amp integrator	1.39
OTRA based integrator	1.14
ICCII based integrator	0.41

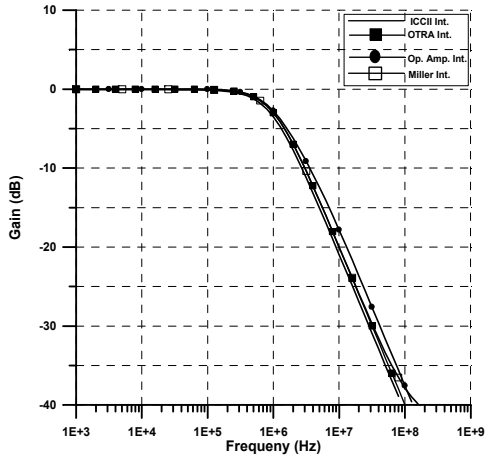

Fig. 26 Frequency responses of the four integrators

As it seen in Table I, Miller integrator has the best THD performance. Table II shows the features of the nonlinearity cancellation techniques [12].

The frequency responses of the four integrators which are mentioned above are shown in Fig. 26.

TABLE II
FEATURES OF THE NONLINEARITY CANCELLATION TECHNIQUES

	Fig. 4	Fig. 5	Fig. 6	Fig. 7
Number of Transistors	1	2	4	2
Cancelling Odd Nonlinearities	Fully	Fully	Fully	Fully
Cancelling Even Nonlinearities	Fully	Fully	Fully	Not Fully

IV. CONCLUSION

In this paper, realization method of passive resistor using MOS transistors and nonlinearity cancellation techniques of MOS transistor current are presented. Four techniques are tested in a sample integrator circuit which is sequentially employing Op-amp, OTRA and ICCII as active elements to do a comparative performance analysis. All of the circuits are implemented by MOS-C realization and simulated by SPICE program using 0.35µm process TSMC MOSIS model parameters. The output waveforms, frequency responses, THD analysis results and features of the nonlinearity cancellation techniques are also given for all circuits taken into comparison. It is shown that these nonlinearity cancellation techniques achieve a good performance and THD values are quite low. Also, all of the circuits have gained electronic tunability by using MOS realization of passive resistors. With MOS-C implementation, the circuits became fully integrable which is very important in IC design.

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